

## XAUI / XGXS Bus Functional Model and Bus Monitor/Checker

### Product Brief

### Language – Verilog

### Supported Protocols:

- 10G Ethernet XAUI
- XGXS

### Transmit Features

- Packet encapsulation and preamble insertion per 802.11
- Ordered set mapping for idle columns
- Idle mapping optionally performed per 802.11
- Idle mapping optionally performed by parameterized directed random selection
- Up to 85 UI programmable bit skew per lane (see 8b10b SERDES)
- Idle error injection not erring packets:
  - Disparity error
  - Code error
  - Spurious code
- Random error injection erring packets:
  - Disparity error
  - Code error
  - Spurious code
- Parameterized minimum align column spacing
- Optionally controlled by XGMII transmit bus

### Receive Features

- Ordered Set mapping and checking
- Column mapping and checking
- Lane deskew
- Packet decapsulation
- Packet protocol sequence checking
  - /S/ start in lane 0
  - Seven preamble Bytes of '55 followed by SFD
  - /T/ termination followed by K28.5 in final column
- Idle mapping checking
  - First idle after terminate is either align or K28.5 per 802.11
  - Every 16-31 Bytes and align column is expected
  - After each align column a sequence column is legal
  - The remaining idles may be K28.5 or Skip columns
- Can be used as stand alone Bus Monitor
- Optionally provides XGMII receive bus

#### Sync State Machine Model and Checking

- Reference implementation of Sync State Machine IEEE 48-7
- Variable FIFO delay models bit skew time and ingress pipe stages
- Checking to 8bit data bus width or 16bit data bus width
- Tracks disparity and code errors (see 8B10B SERDES)
- Checks DUT 8B10B decoding and error reporting
- Reports Sync Status
- Reports Decoded word
- Reports Disparity and Code error indications

#### Alignment State Machine Model and Checking

- Reference implementation of Alignment State Machine IEEE 48-8
- Variable FIFO delay models bit skew time, ingress pipe stages, and alignment latency
- Checking to 32bit data bus width or 64bit data bus width
- Responds to Sync Status indications as well as ordered sets per lane

#### XGMII Receive State Machine Model and Checking

- Reference implementation of Receive State Machine IEEE 48-9
- Checking to 32bit data bus width or 64bit data bus width
- Responds to Align Status indications as well as aligned columns
- Checks error mapping to /E/
- Checks check\_end function
- Checks Idle mapping in Terminate column
- Checks Idle mapping for Idle columns

#### General Features

- Standard error reporting through common code
- XGMII loopback module included